FIG. 1A
PRIOR ART

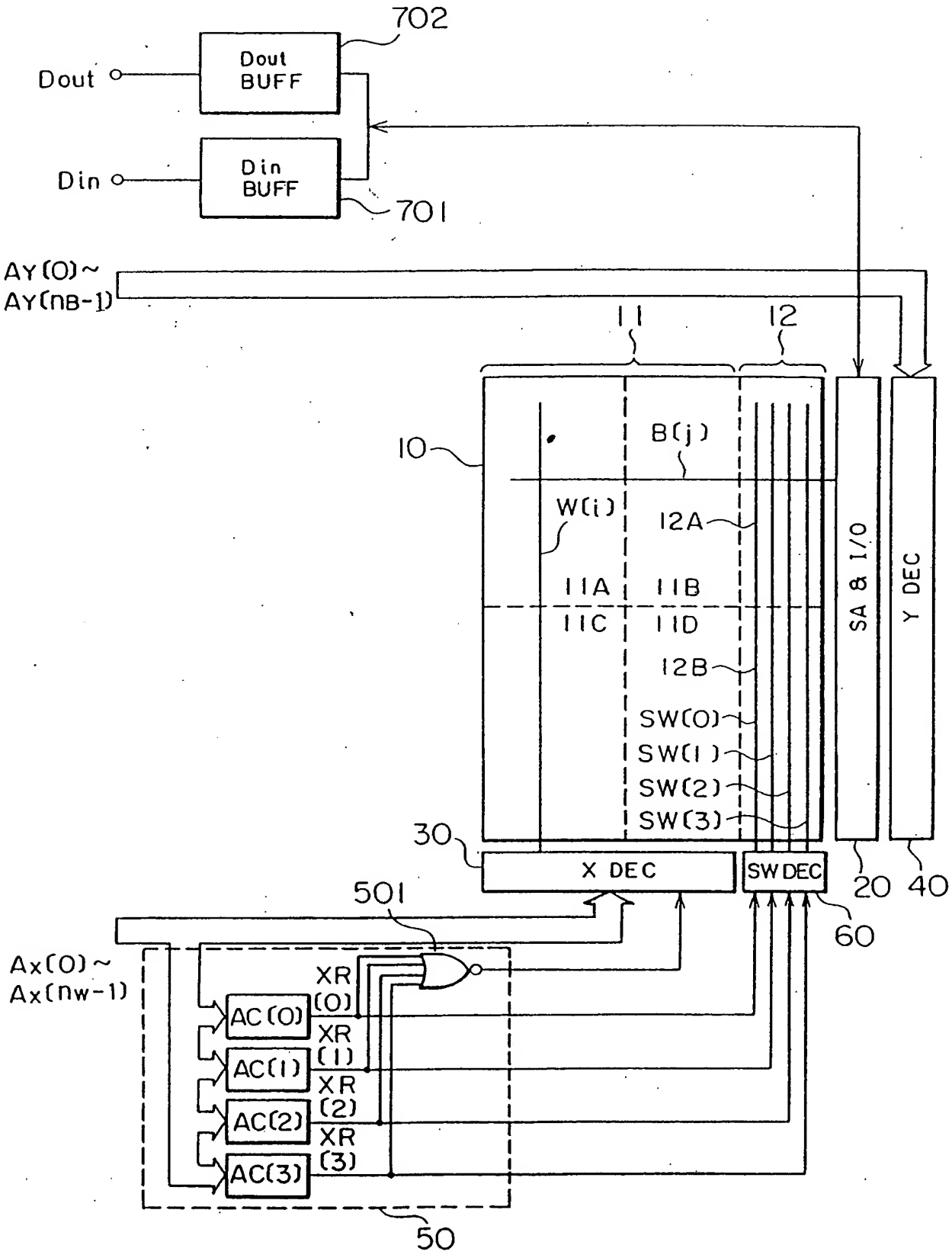


FIG. 1B
PRIOR ART

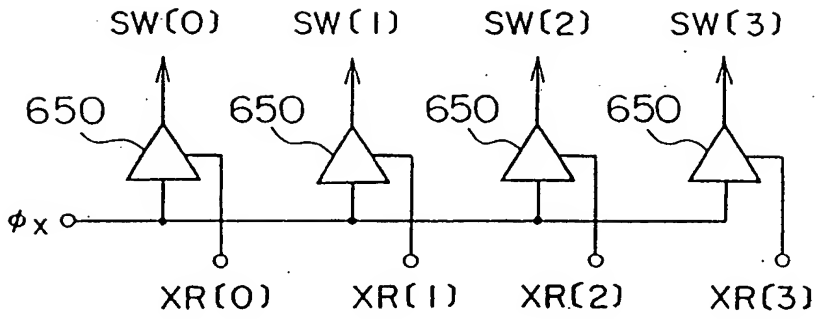


FIG. 2A
PRIOR ART

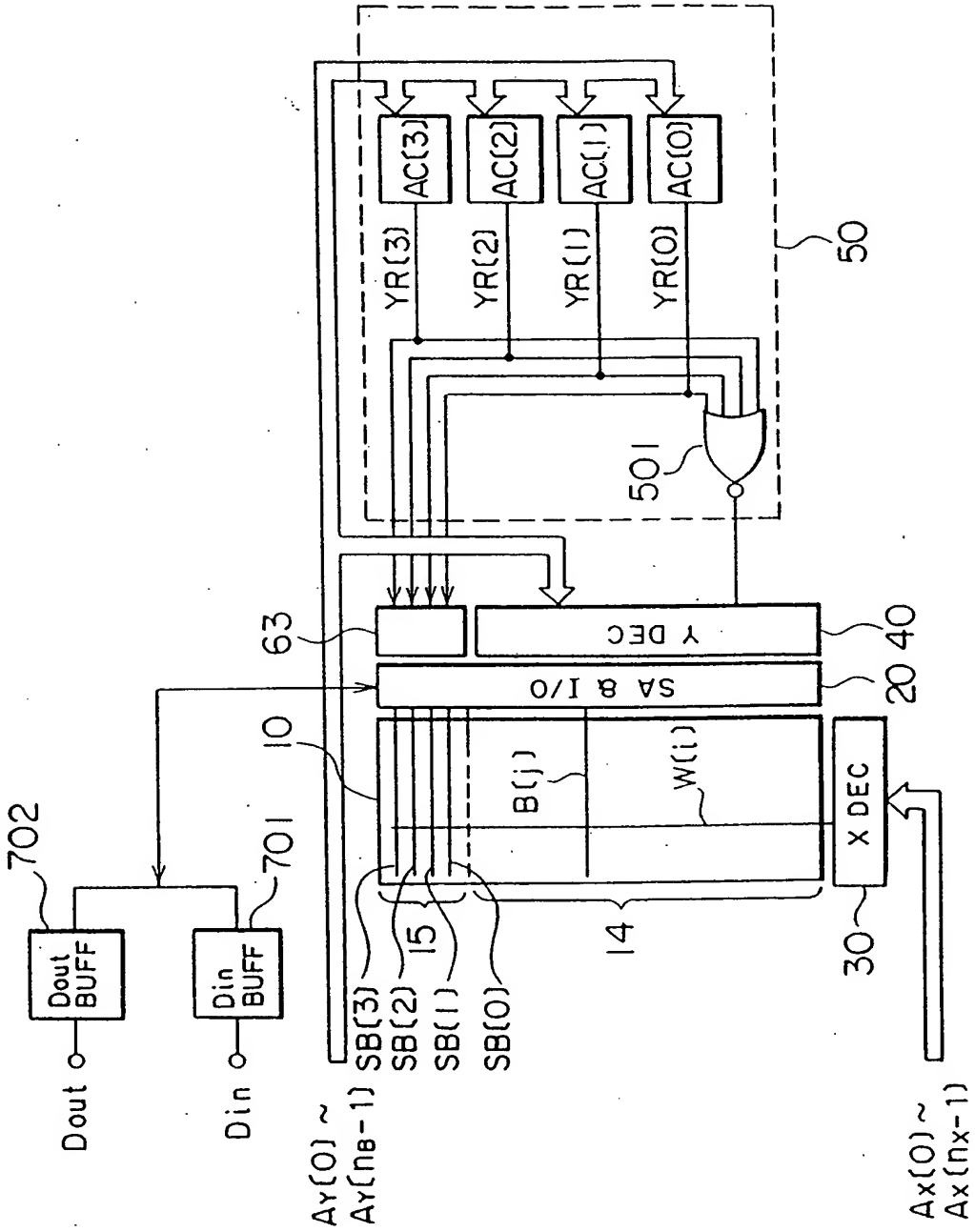


FIG. 2B
PRIOR ART

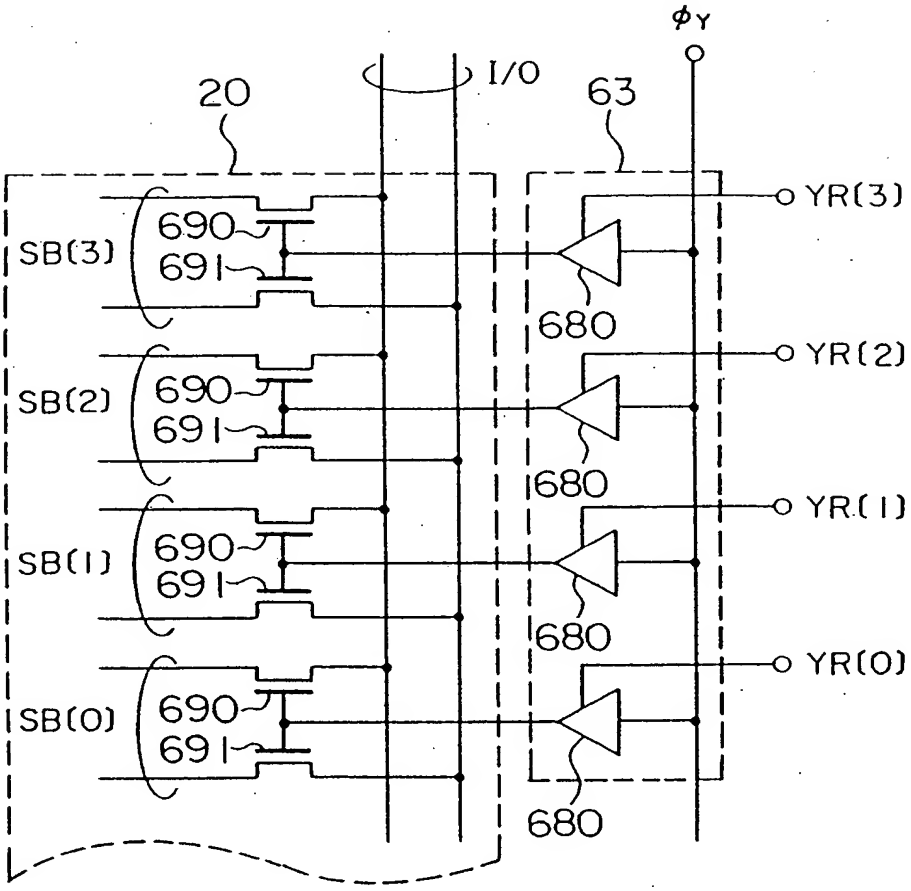


FIG. 3
PRIOR ART

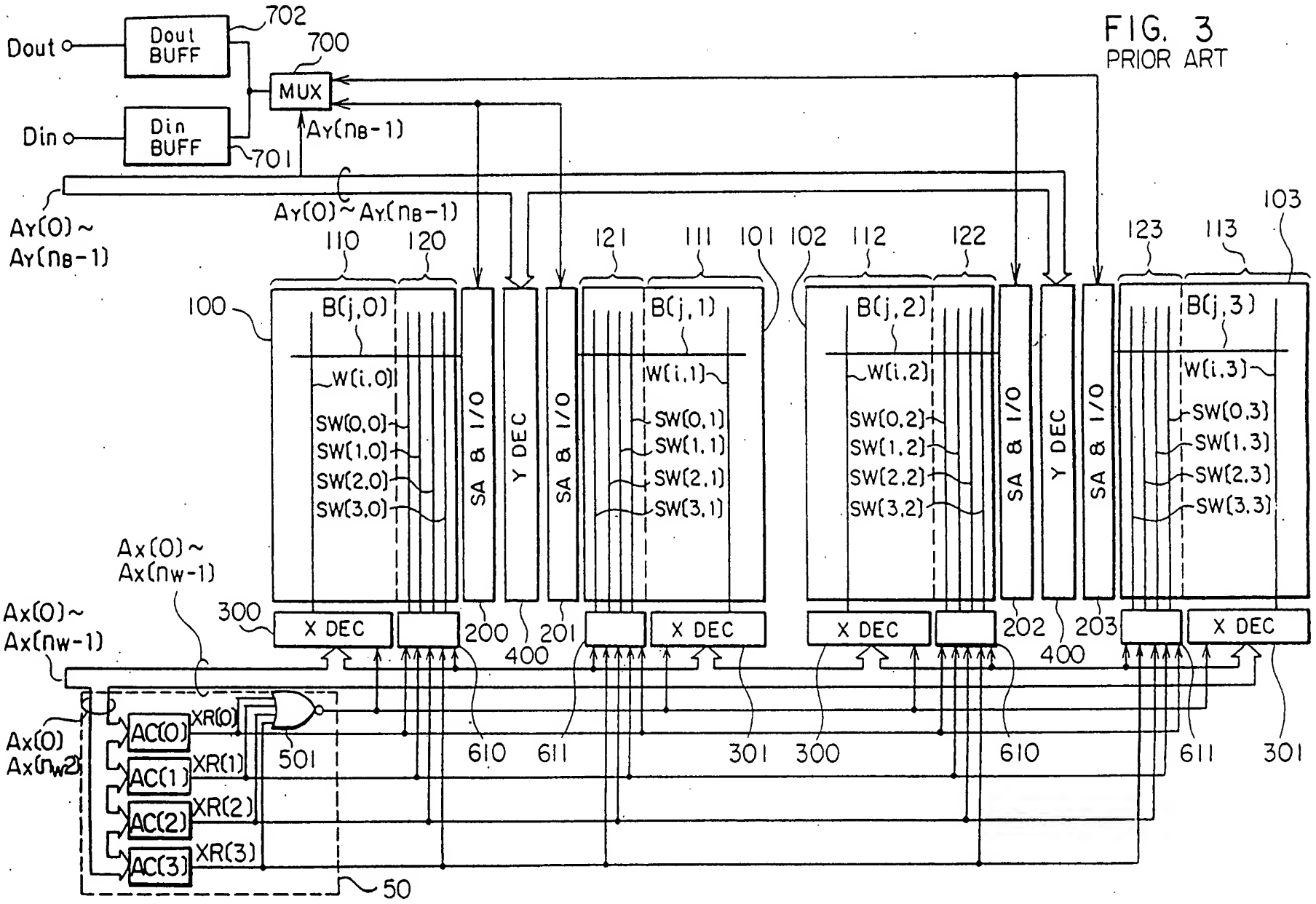


FIG. 4
PRIOR ART

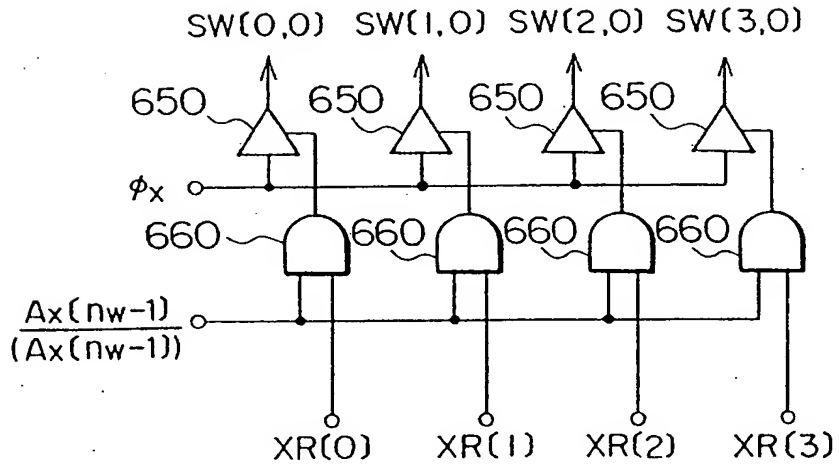


FIG. 5
PRIOR ART

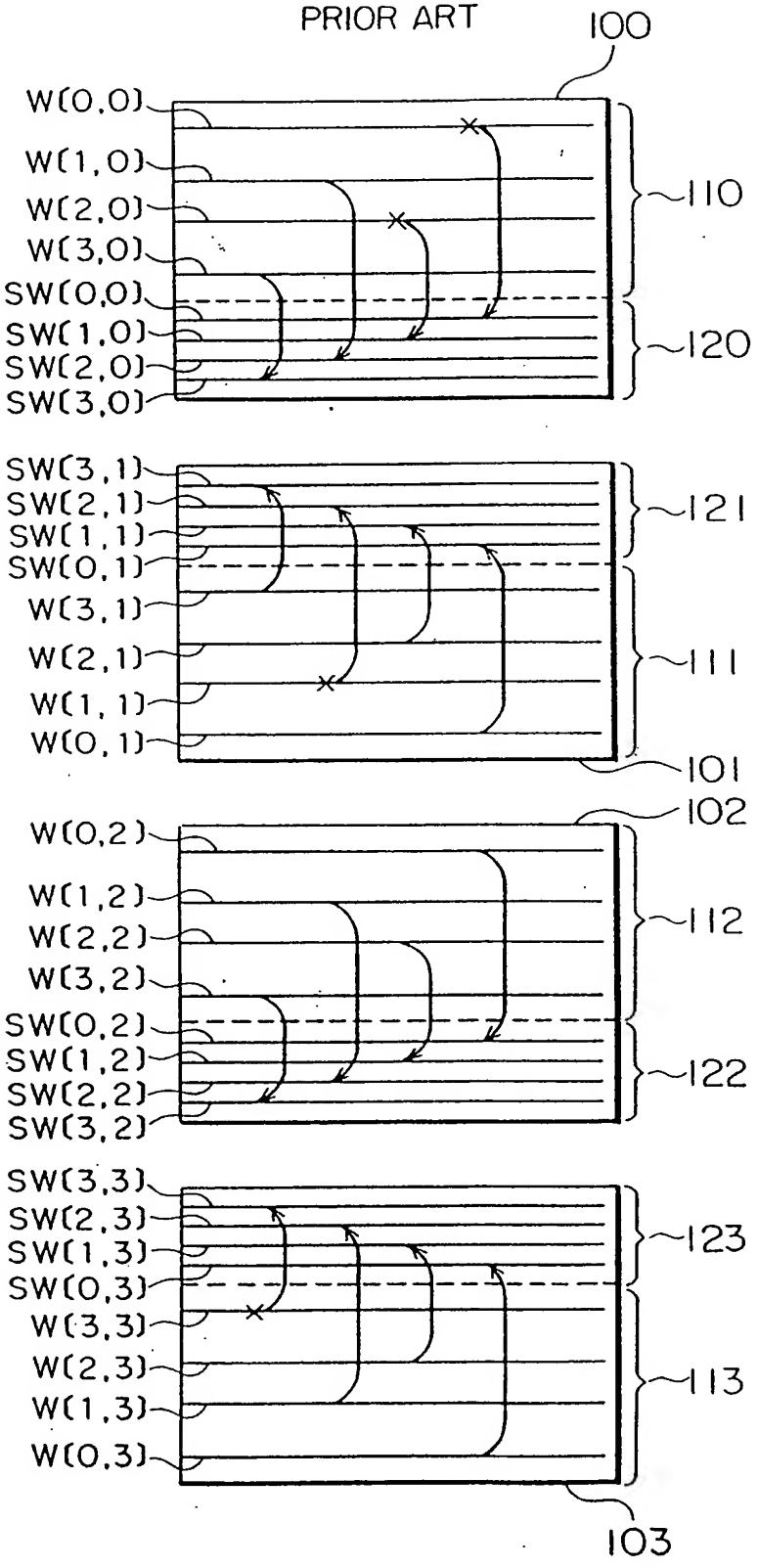


FIG. 6
PRIOR ART

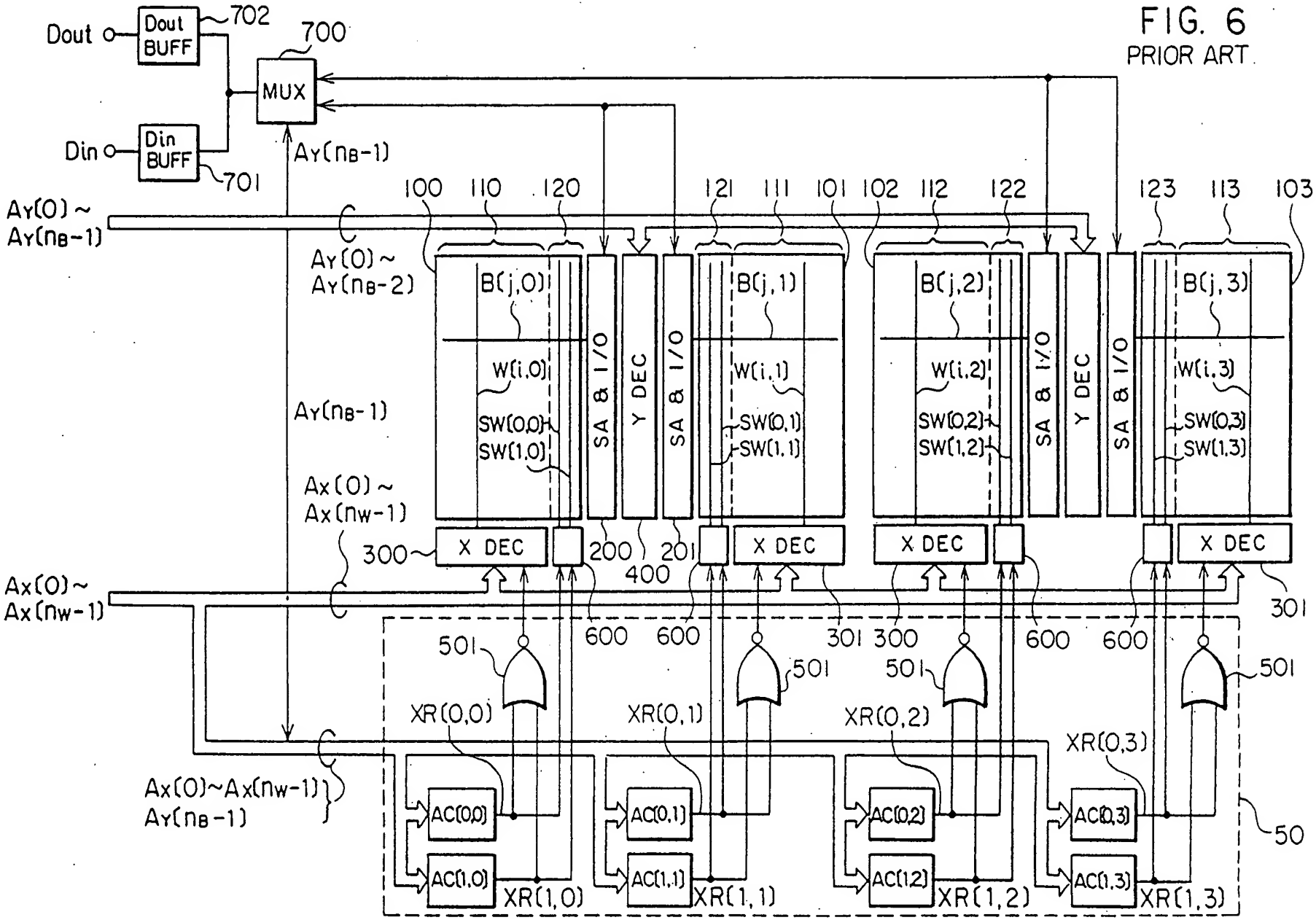


FIG. 7
PRIOR ART

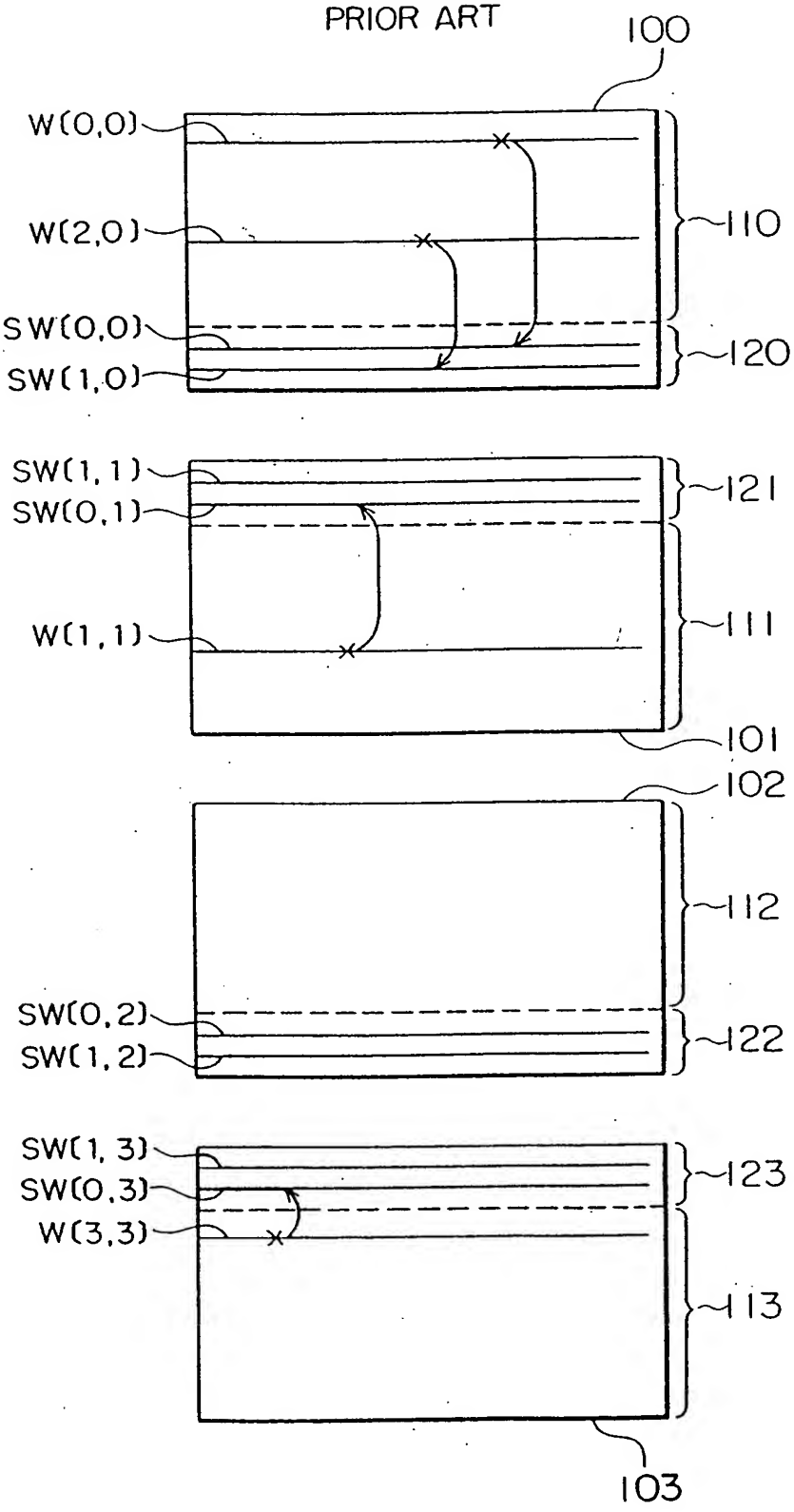


FIG. 8
PRIOR ART

VALUE STORED IN ADDRESS COMPARE CIRCUIT	INPUT ADDRESS	RESULT OF COMPARISON
"0"	"0"	COINCIDENT
	"1"	NOT COINCIDENT
"1"	"0"	NOT COINCIDENT
	"1"	COINCIDENT
"X"	"0"	COINCIDENT
	"1"	COINCIDENT

FIG. 9

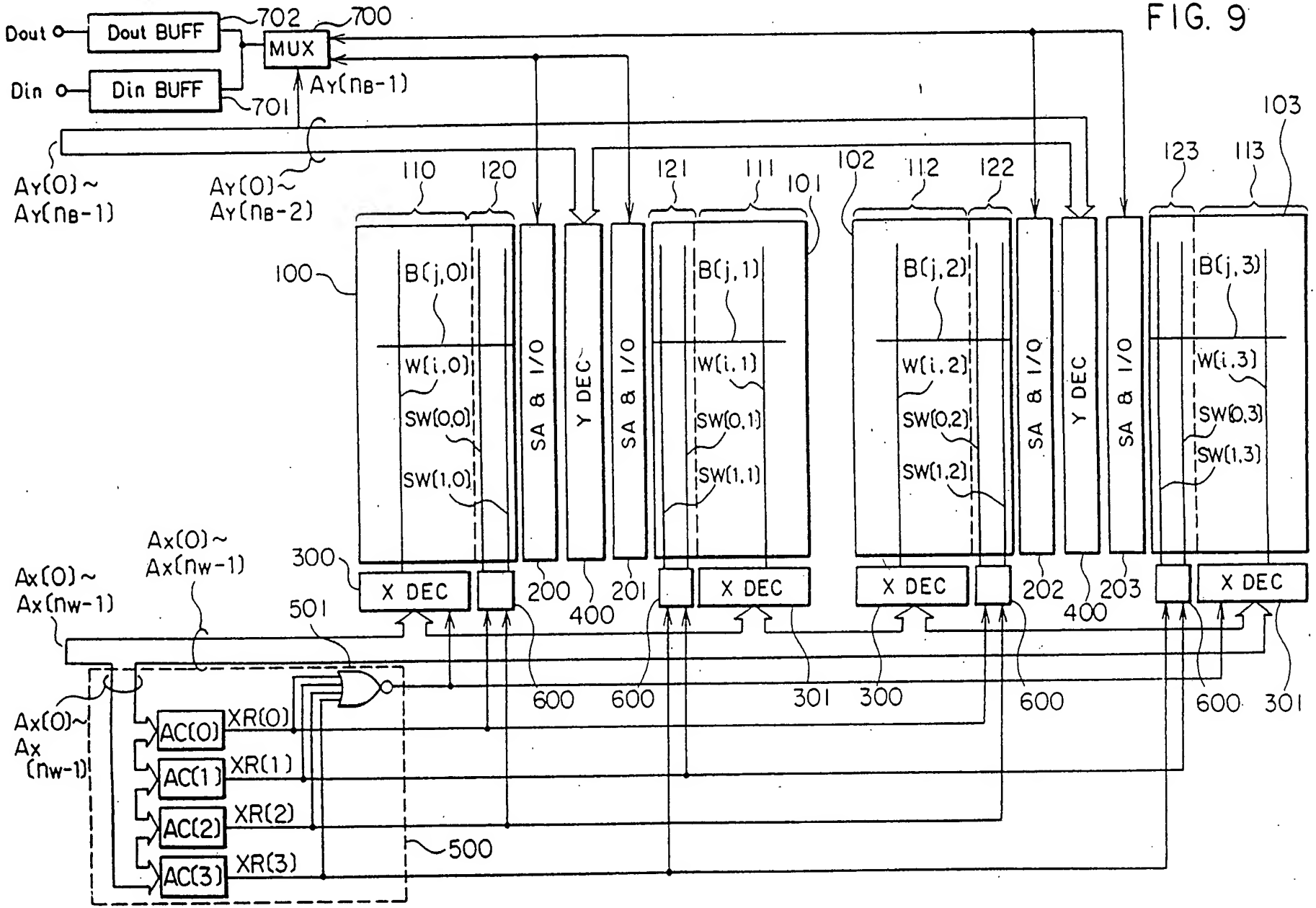

Dout
Dout BUFF
702
700
MUX
Din
Din BUFF
701
AY(nB-1)
AY(0)~
AY(nB-1)
AY(0)~
AY(nB-2)
110
120
121
111
101
102
112
122
123
113
103
100
B(j,0)
B(j,1)
B(j,2)
B(j,3)
W(i,0)
W(i,1)
W(i,2)
W(i,3)
SW(0,0)
SW(1,0)
SW(0,1)
SW(1,1)
SW(0,2)
SW(1,2)
SW(0,3)
SW(1,3)
SA & I/O
Y DEC
SA & I/O
SA & I/O
Y DEC
SA & I/O
300
X DEC
X DEC
X DEC
X DEC
200
201
202
203
400
400
501
Ax(0)~
Ax(nw-1)
Ax(0)~
Ax(nw-1)
Ax(0)~
Ax
(nw-1)
AC(0)
AC(1)
AC(2)
AC(3)
XR(0)
XR(1)
XR(2)
XR(3)
500
600
600
301
300
600
600
301

FIG. 10

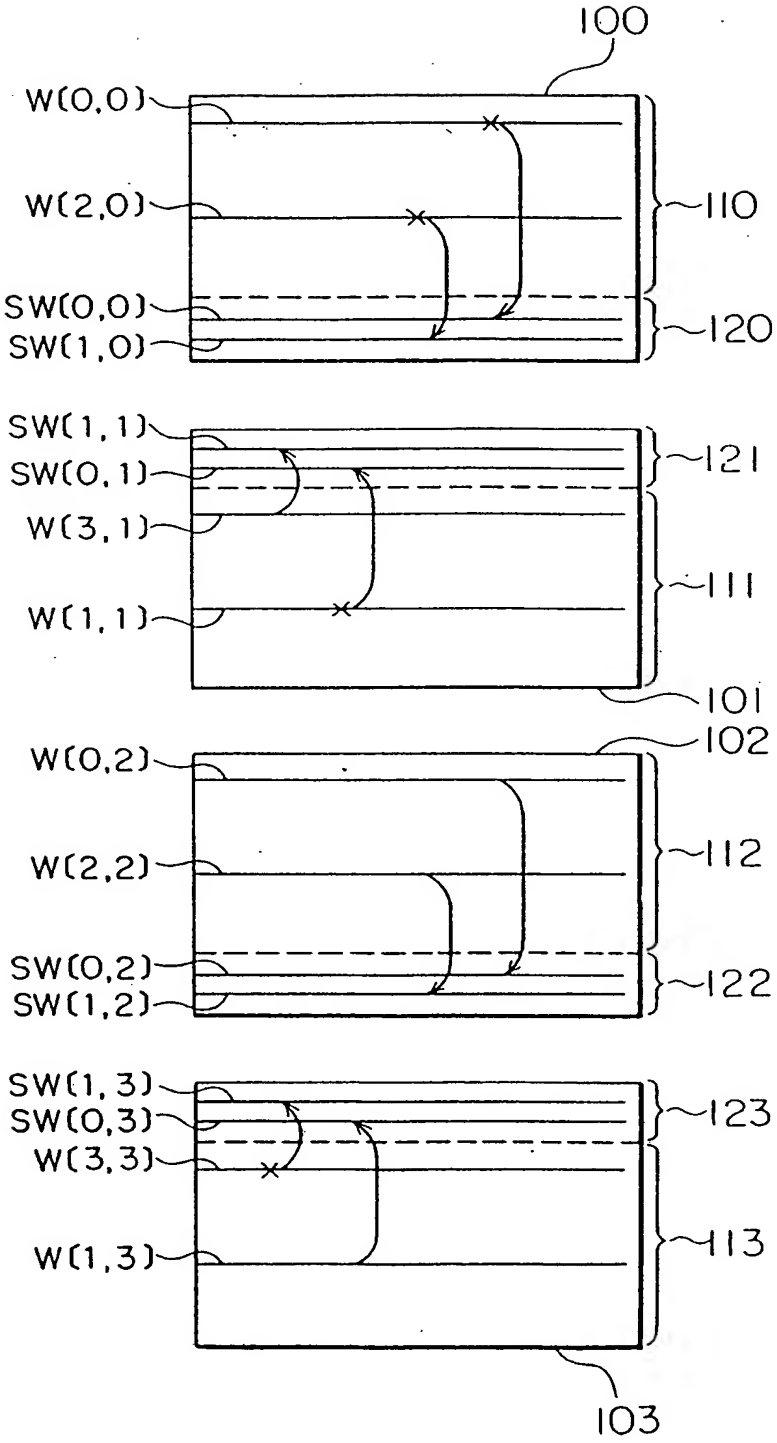

100
W(0,0)
W(2,0)
110
SW(0,0)
SW(1,0)
120
SW(1,1)
SW(0,1)
121
W(3,1)
111
W(1,1)
101
102
W(0,2)
W(2,2)
112
SW(0,2)
SW(1,2)
122
SW(1,3)
SW(0,3)
123
W(3,3)
W(1,3)
113
103

FIG. 11

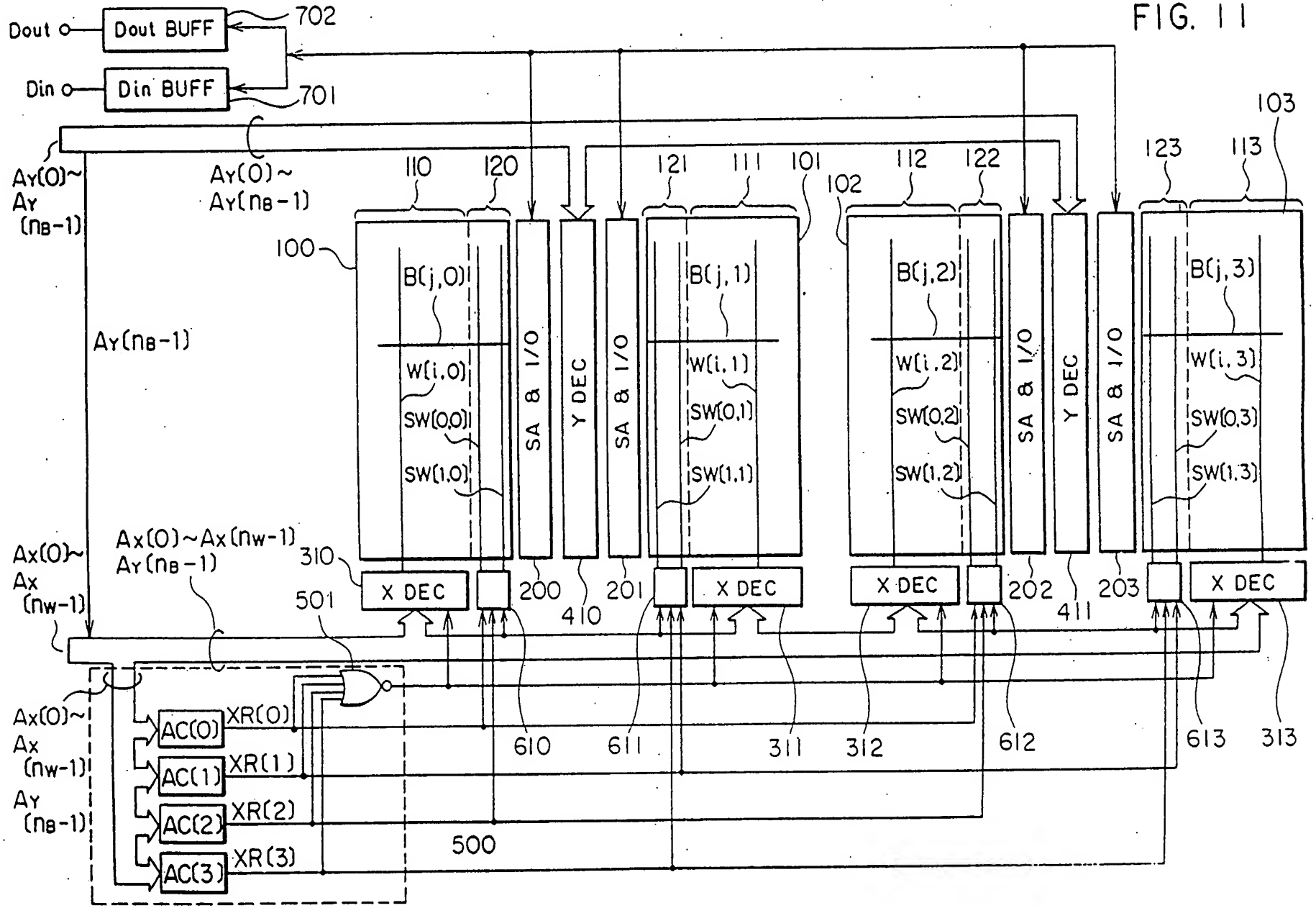

Dout
Dout BUFF
702
Din
Din BUFF
701
103
Ay(0)~
Ay
(nB-1)
Ay(0)~
Ay(nB-1)
110
120
121
111
101
102
112
122
123
113
100
B(j,0)
B(j,1)
B(j,2)
B(j,3)
Ay(nB-1)
W(i,0)
W(i,1)
W(i,2)
W(i,3)
SW(0,0)
SW(0,1)
SW(0,2)
SW(0,3)
SW(1,0)
SW(1,1)
SW(1,2)
SW(1,3)
SA & I/O
Y DEC
SA & I/O
SA & I/O
Y DEC
SA & I/O
Ax(0)~
Ax
(nw-1)
Ax(0)~Ax(nw-1)
Ay(nB-1)
310
X DEC
X DEC
X DEC
X DEC
501
200
201
202
203
410
411
Ax(0)~
Ax
(nw-1)
Ay
(nB-1)
AC(0)
AC(1)
AC(2)
AC(3)
XR(0)
XR(1)
XR(2)
XR(3)
610
611
311
312
612
613
313
500

FIG. 12

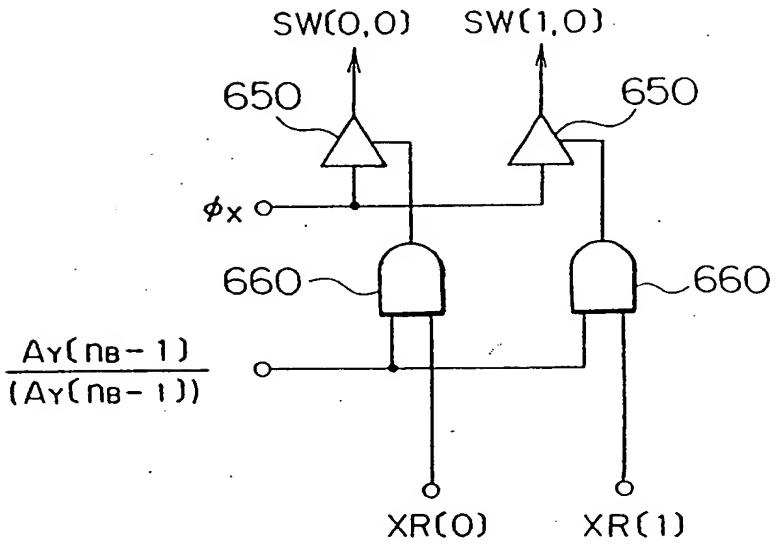


FIG. 13

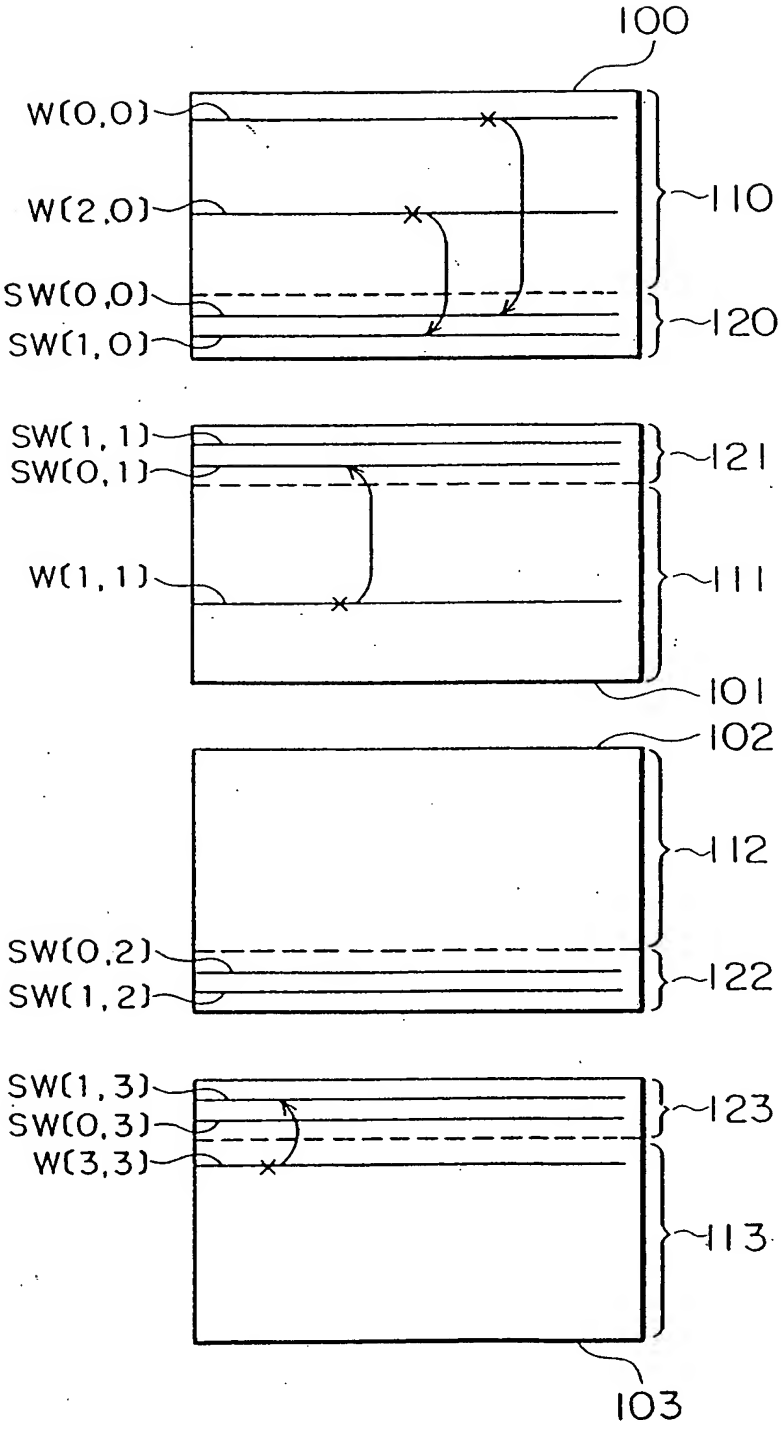

100
W(0,0)
W(2,0)
SW(0,0)
SW(1,0)
110
120
SW(1,1)
SW(0,1)
W(1,1)
121
111
101
102
112
SW(0,2)
SW(1,2)
122
SW(1,3)
SW(0,3)
W(3,3)
123
113
103

FIG. 14

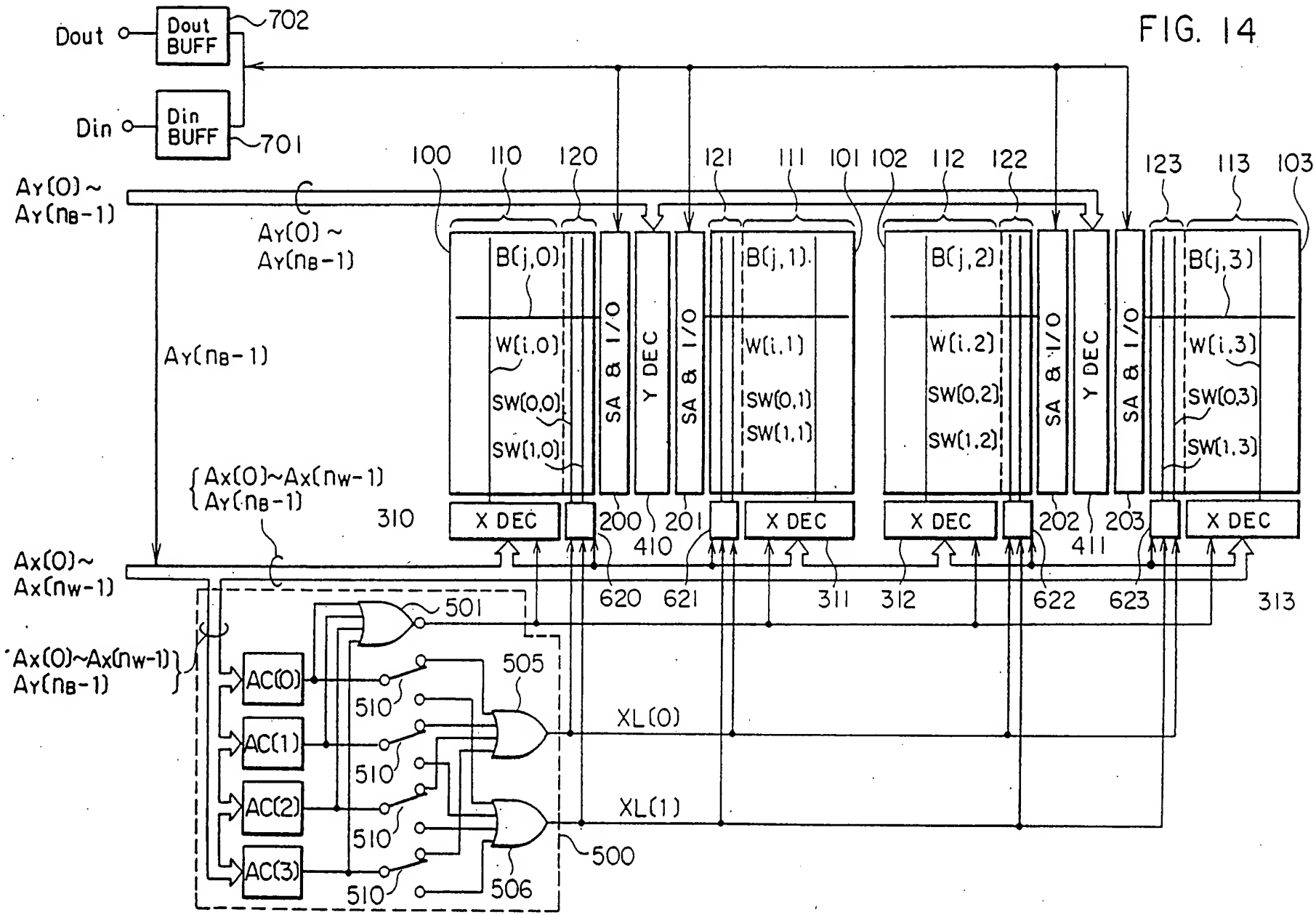

Dout
Dout BUFF
702
Din
Din BUFF
701
Ay(0)~Ay(nB-1)
Ay(nB-1)
100
110
120
121
111
101
102
112
122
123
113
103
B(j,0)
B(j,1)
B(j,2)
B(j,3)
W(i,0)
W(i,1)
W(i,2)
W(i,3)
SW(0,0)
SW(1,0)
SW(0,1)
SW(1,1)
SW(0,2)
SW(1,2)
SW(0,3)
SW(1,3)
SA & I/O
Y DEC
X DEC
{Ax(0)~Ax(nw-1) Ay(nB-1)
310
200
201
202
203
410
411
Ax(0)~Ax(nw-1)
620
621
311
312
622
623
313
501
505
AC(0)
AC(1)
AC(2)
AC(3)
510
XL(0)
XL(1)
500
506

FIG. 15

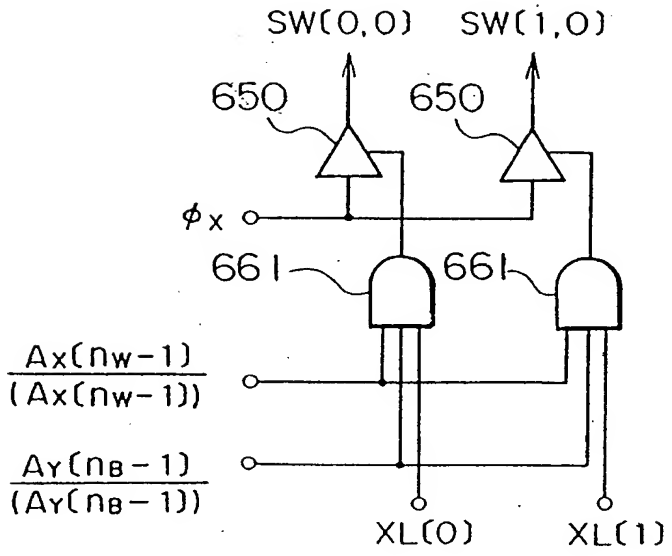

SW(0,0)
SW(1,0)
650
650
φx
661
661
Ax(nw-1)
(Ax(nw-1))
AY(nB-1)
(AY(nB-1))
XL(0)
XL(1)

FIG. 16

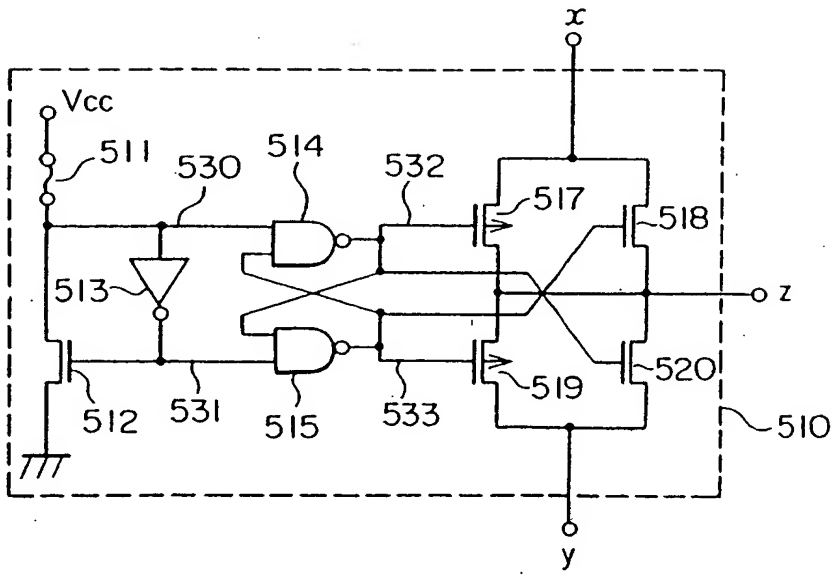

x
Vcc
511
530
514
532
517
518
513
z
512
531
515
533
519
520
510
y

FIG. 17

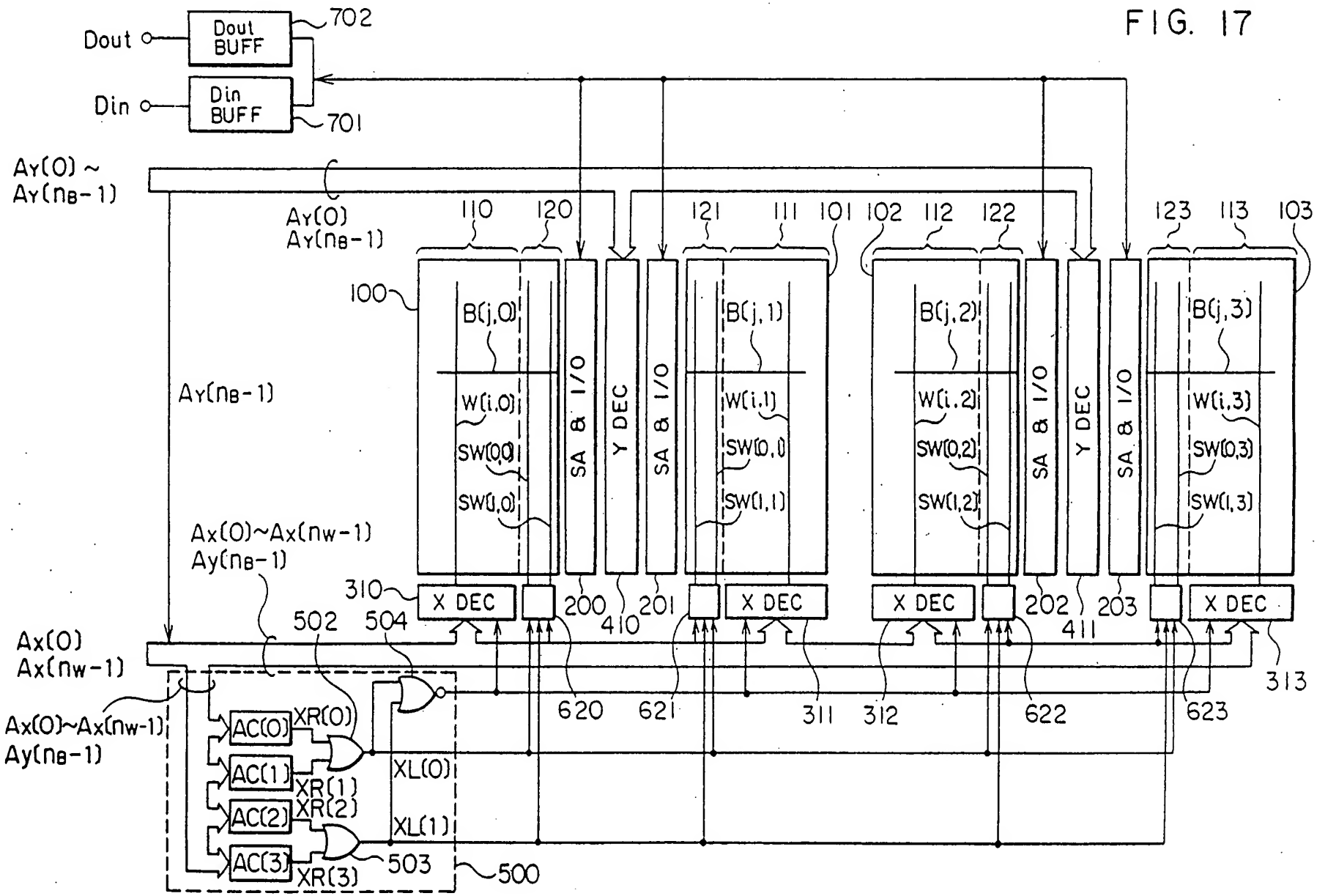

Dout
Dout BUFF
702
Din
Din BUFF
701
Ay(0) ~ Ay(nB-1)
Ay(0)
Ay(nB-1)
110
120
121
111
101
102
112
122
123
113
103
100
B(j,0)
B(j,1)
B(j,2)
B(j,3)
W(i,0)
W(i,1)
W(i,2)
W(i,3)
SW(0,0)
SW(1,0)
SW(0,1)
SW(1,1)
SW(0,2)
SW(1,2)
SW(0,3)
SW(1,3)
SA & I/O
Y DEC
Ay(nB-1)
Ax(0)~Ax(nw-1)
Ay(nB-1)
310
X DEC
200
410
201
202
411
203
502
504
Ax(0)
Ax(nw-1)
620
621
311
312
622
623
313
Ax(0)~Ax(nw-1)
Ay(nB-1)
AC(0)
AC(1)
AC(2)
AC(3)
XR(0)
XR(1)
XR(2)
XR(3)
XL(0)
XL(1)
503
500

FIG. 18

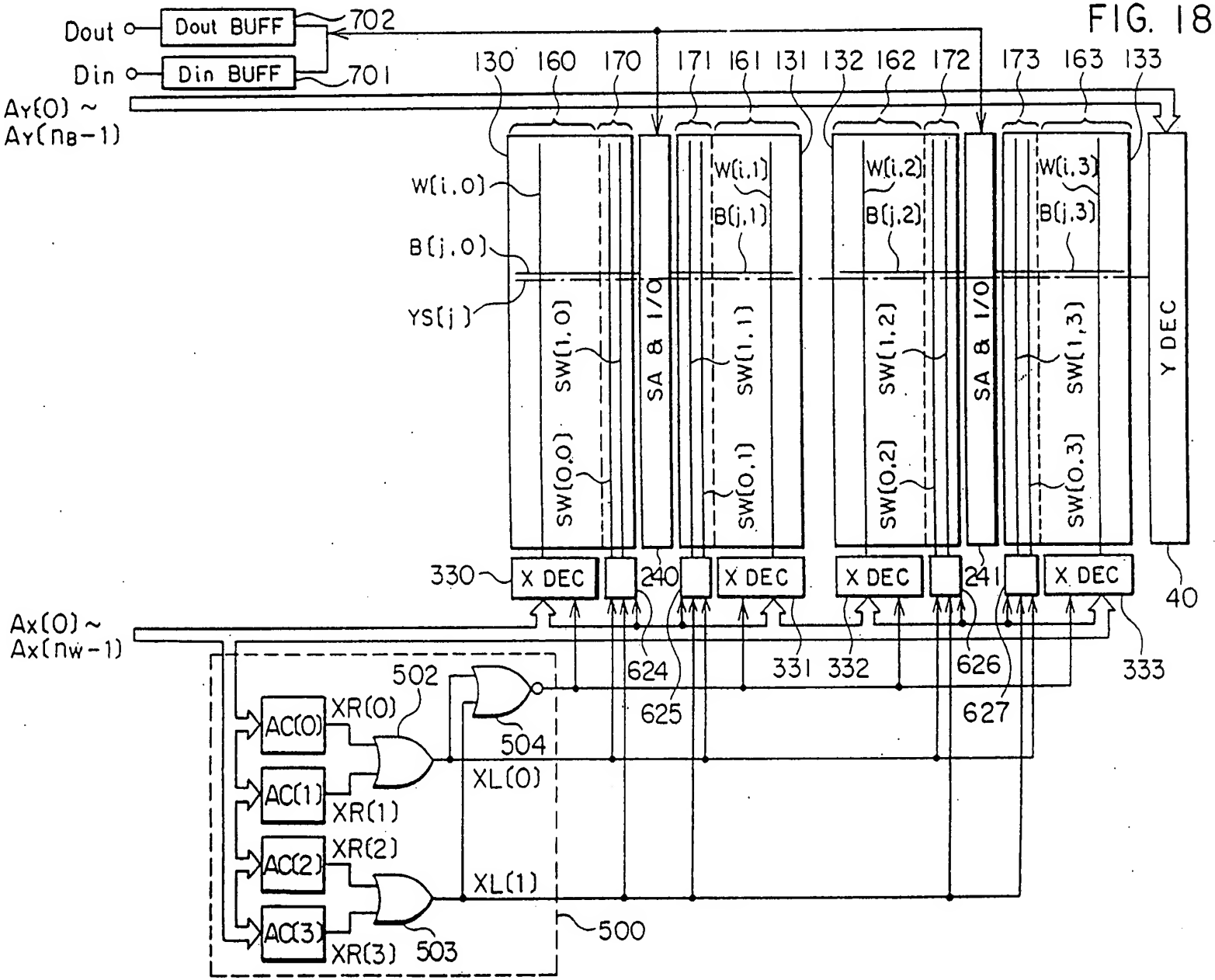

Dout
Dout BUFF
702
Din
Din BUFF
701
AY(0) ~
AY(nB-1)
130 160 170 171 161 131 132 162 172 173 163 133
W(i,0)
B(j,0)
YS(j)
W(i,1)
B(j,1)
W(i,2)
B(j,2)
W(i,3)
B(j,3)
SW(0,0)
SW(1,0)
SA & I/O
SW(0,1)
SW(1,1)
SW(0,2)
SW(1,2)
SA & I/O
SW(0,3)
SW(1,3)
Y DEC
40
330
X DEC
240
X DEC
X DEC
241
X DEC
Ax(0) ~
Ax(nw-1)
624
625
331
332
626
627
333
502
504
AC(0)
XR(0)
AC(1)
XR(1)
XL(0)
AC(2)
XR(2)
AC(3)
XR(3)
503
XL(1)
500

FIG. 19

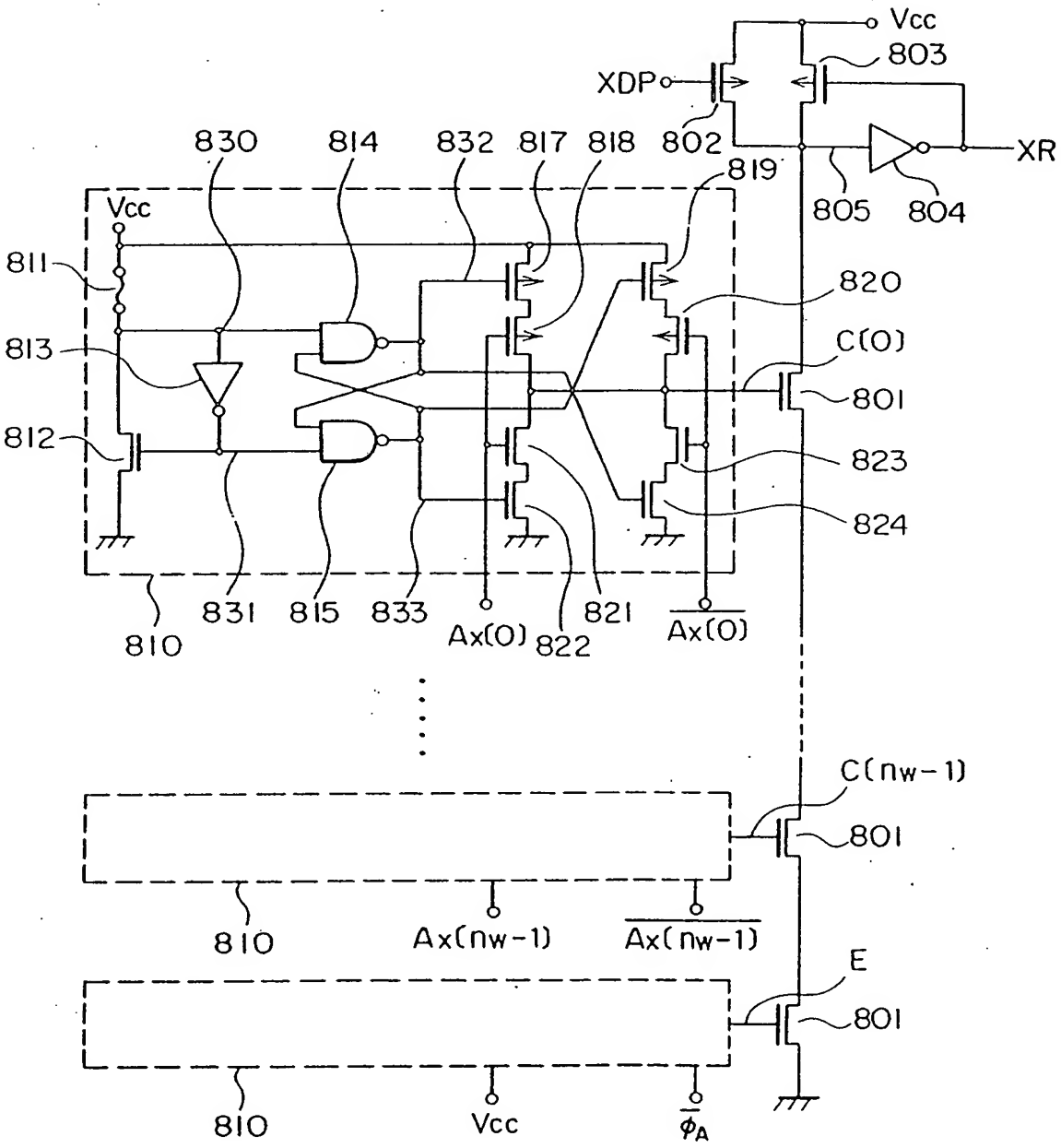

Vcc
803
XDP
802
XR
805
804
830
814
832
817
818
819
811
813
812
820
C(0)
801
823
824
831
815
833
Ax(0)
822
821
$\overline{Ax(0)}$
810
C(nw-1)
801
810
Ax(nw-1)
$\overline{Ax(nw-1)}$
E
801
810
Vcc
$\overline{\phi_A}$

FIG. 20

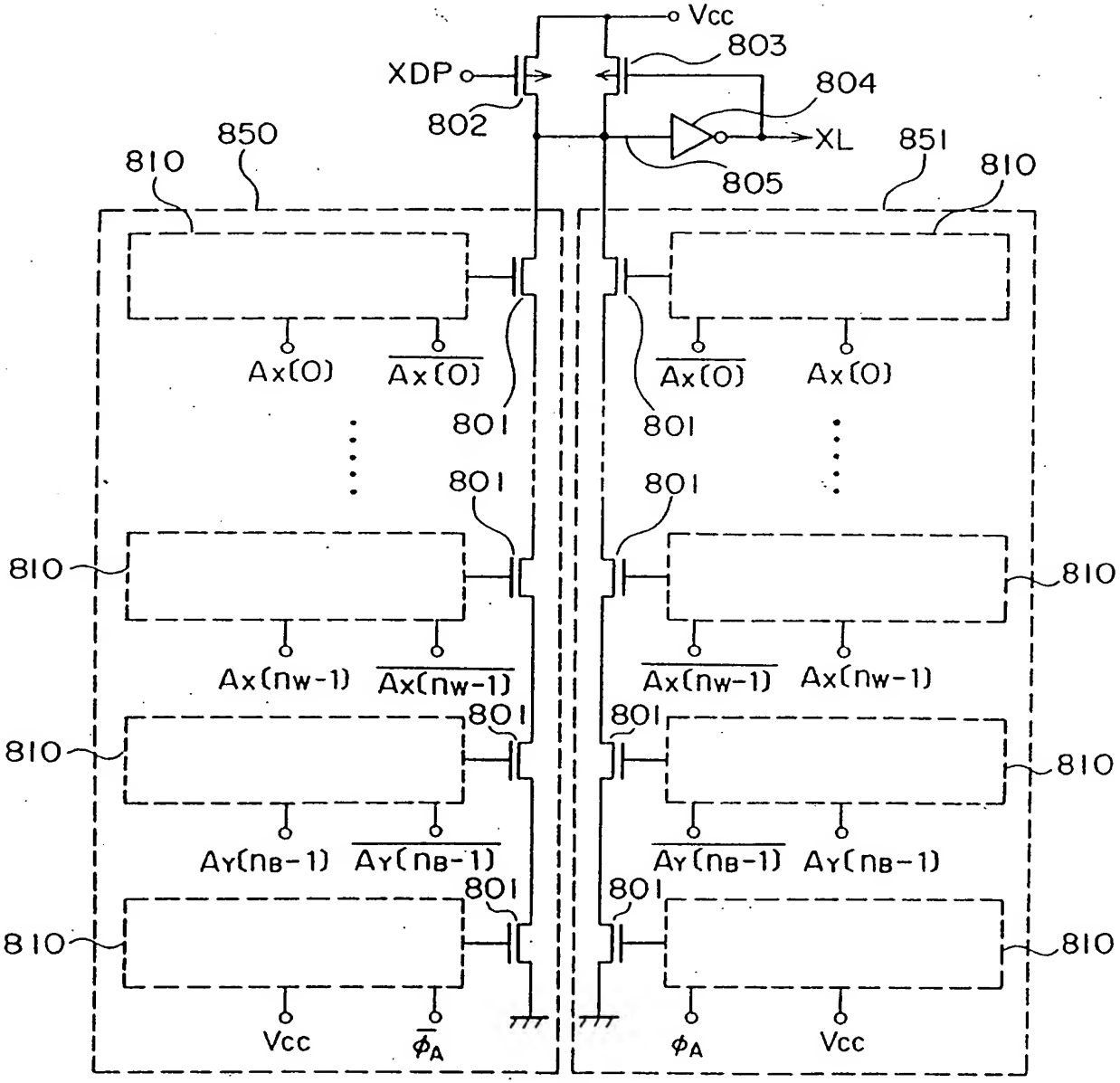

Vcc
803
XDP
804
802
XL
850
851
805
810
810
Ax(0)
Ax(0)
Ax(0)
Ax(0)
801
801
801
801
810
810
Ax(nw-1)
Ax(nw-1)
Ax(nw-1)
Ax(nw-1)
801
801
810
810
AY(nB-1)
AY(nB-1)
AY(nB-1)
AY(nB-1)
801
801
810
810
Vcc
$\overline{\phi_A}$
ϕ_A
Vcc

FIG. 21

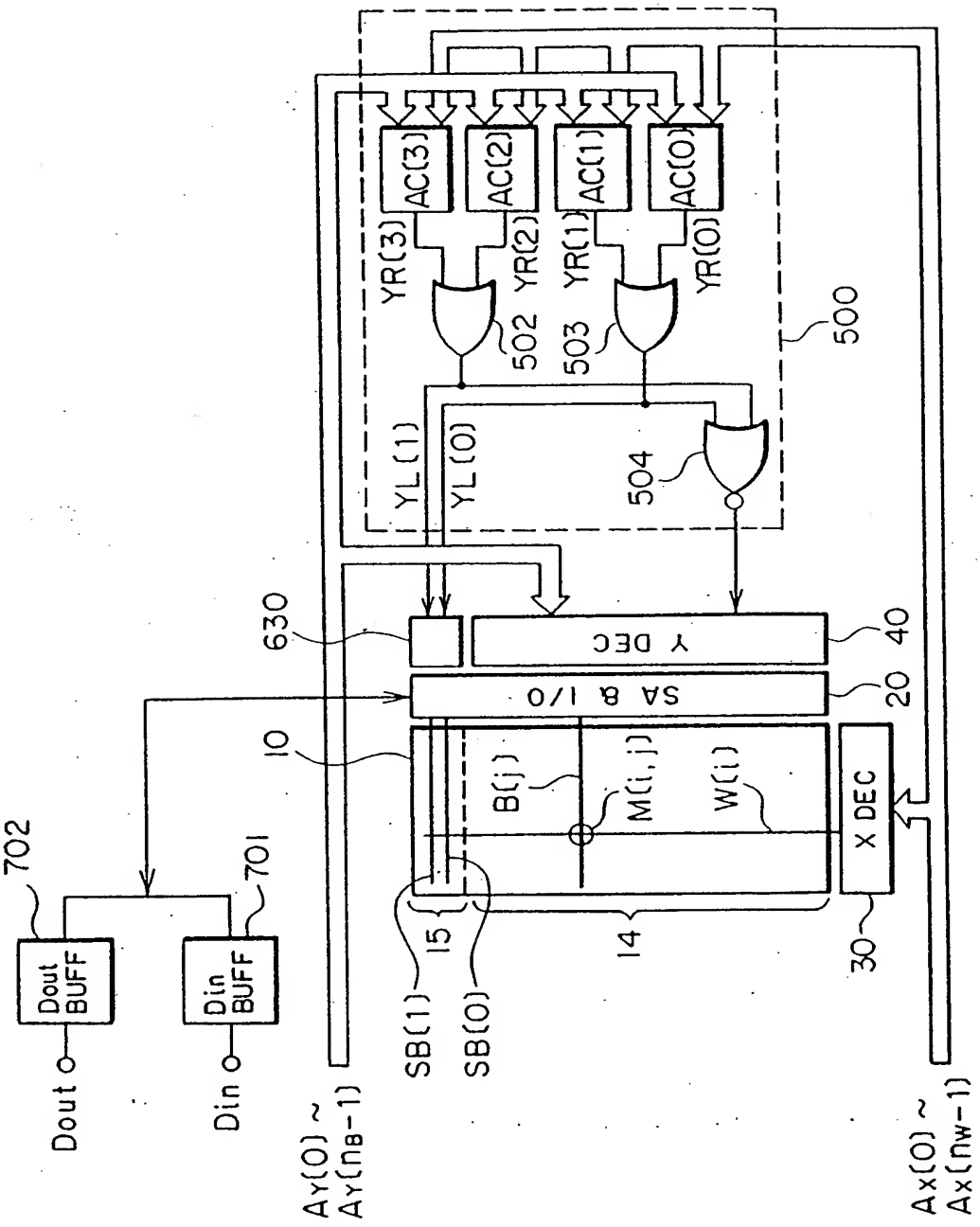

AC(3)
AC(2)
AC(1)
AC(0)
YR(3)
YR(2)
YR(1)
YR(0)
502
503
504
500
YL(1)
YL(0)
630
Y DEC
40
SA & I/O
20
10
B(j)
M(i,j)
W(i)
X DEC
15
14
30
SB(1)
SB(0)
702
701
Dout BUFF
Din BUFF
Dout
Din
Ay(0) ~ Ay(nB-1)
Ax(0) ~ Ax(nw-1)

FIG. 22

ADDRESS		COMPARED / NOT COMPARED		
ROW ADDRESS	$A_X(0)$	○	×	×
	$A_X(1)$	○	○	×
	$A_X(2)$	○	○	×
	⋮	⋮	⋮	⋮
	$A_X(n_W-3)$	○	○	×
	$A_X(n_W-2)$	○	○	×
	$A_X(n_W-1)$	○	○	×
COLUMN ADDRESS	$A_Y(0)$	○	○	○
	$A_Y(1)$	○	○	○
	$A_Y(2)$	○	○	○
	⋮	⋮	⋮	⋮
	$A_Y(n_B-3)$	○	○	○
	$A_Y(n_B-2)$	○	○	○
	$A_Y(n_B-1)$	○	○	○
NUMBER OF BITS REPLACED AT A TIME		1	2	N_W

○ : COMPARED

× : NOT COMPARED

FIG. 23

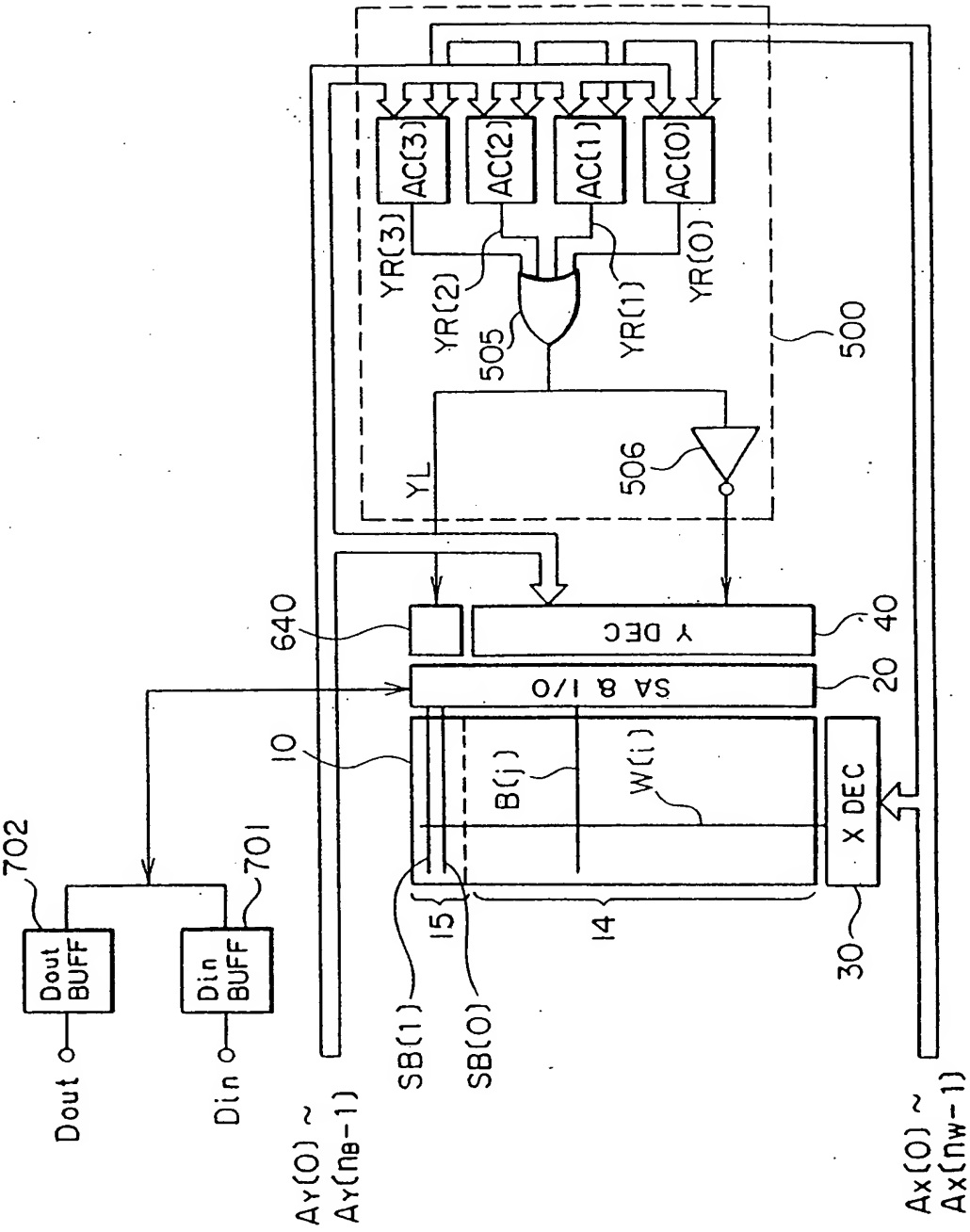

AC(3)
AC(2)
AC(1)
AC(0)
YR(3)
YR(2)
YR(1)
YR(0)
505
500
YL
506
640
Y DEC
40
SA & I/O
20
10
B(j)
W(i)
X DEC
15
14
30
SB(1)
SB(0)
702
701
Dout BUFF
Din BUFF
Dout
Din
Ay(0) ~ Ay(nB-1)
Ax(0) ~ Ax(nw-1)

FIG. 24A

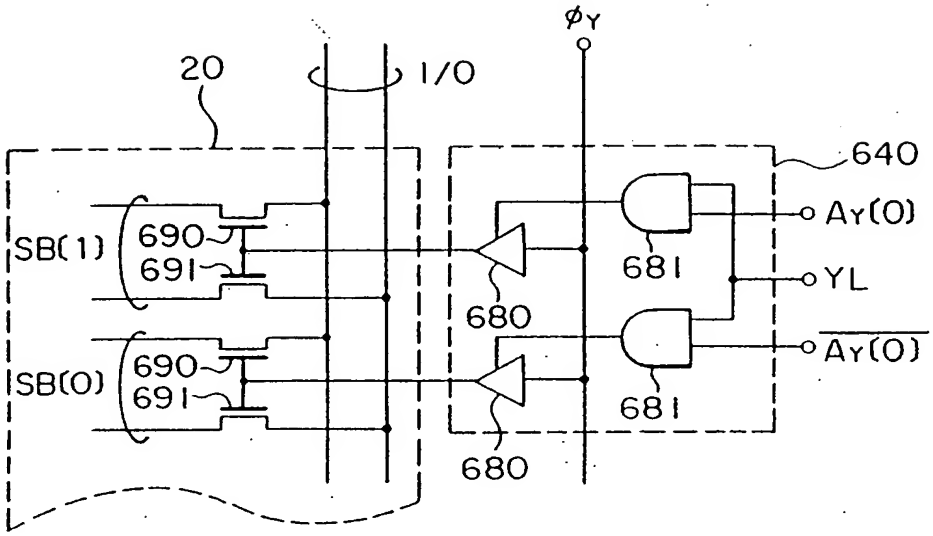


FIG. 24B

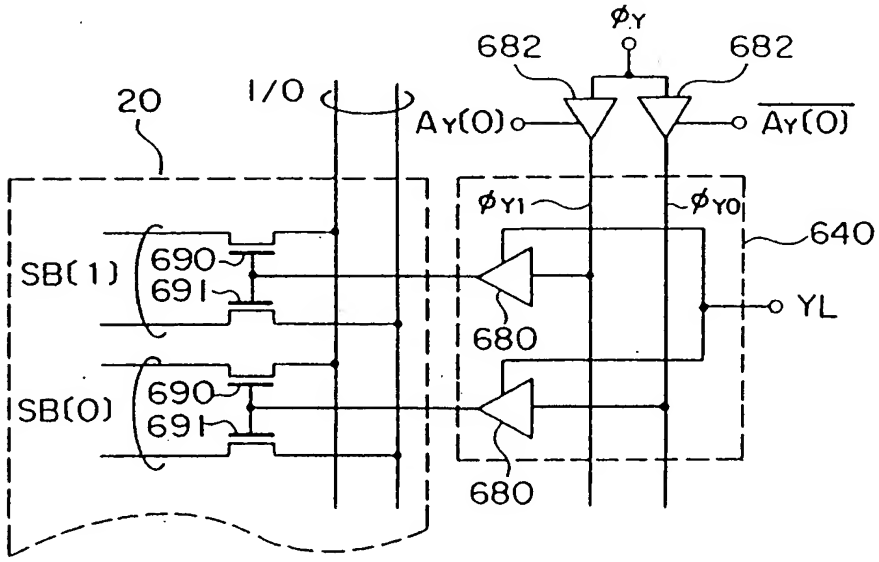


FIG. 25

ADDRESS		COMPARED / NOT COMPARED					
ROW ADDRESS	$A_X(0)$	○	×	○	×	×	×
	$A_X(1)$	○	○	○	○	×	×
	$A_X(2)$	○	○	○	○	×	×
	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	$A_X(n_W-3)$	○	○	○	○	×	×
	$A_X(n_W-2)$	○	○	○	○	×	×
	$A_X(n_W-1)$	○	○	○	○	×	×
COLUMN ADDRESS	$A_Y(0)$	○	○	×	×	○	×
	$A_Y(1)$	○	○	○	○	○	○
	$A_Y(2)$	○	○	○	○	○	○
	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	$A_Y(n_B-3)$	○	○	○	○	○	○
	$A_Y(n_B-2)$	○	○	○	○	○	○
	$A_Y(n_B-1)$	○	○	○	○	○	○
NUMBER OF BITS REPLACED AT A TIME		1	2	2	4	Nw	2Nw

○ : COMPARED
× : NOT COMPARED

FIG. 26

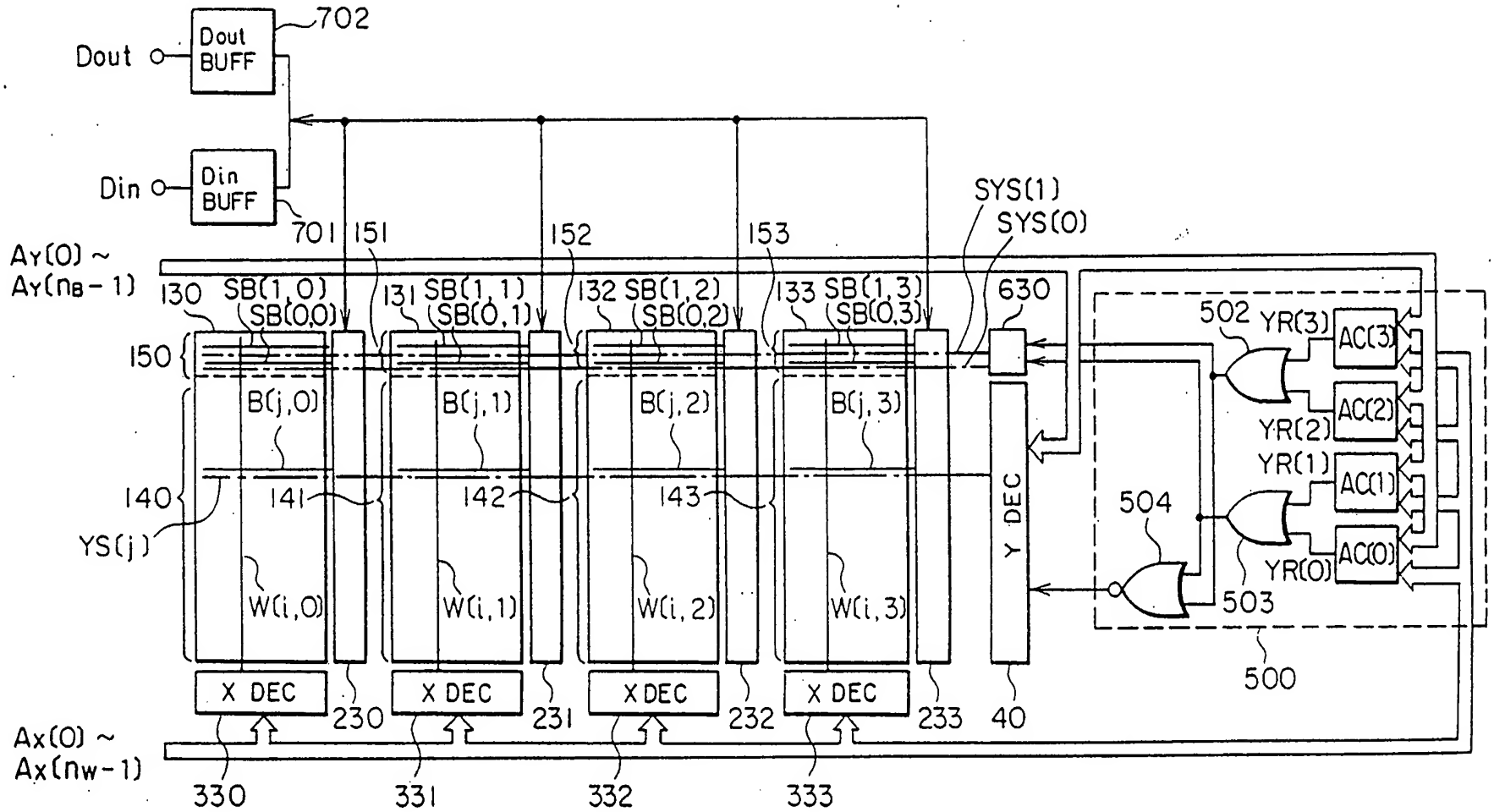

Dout
Dout BUFF
702
Din
Din BUFF
701
151
152
153
SYS(1)
SYS(0)
Ay(0) ~ Ay(nB-1)
130
SB(1,0)
SB(0,0)
131
SB(1,1)
SB(0,1)
132
SB(1,2)
SB(0,2)
133
SB(1,3)
SB(0,3)
630
150
B(j,0)
B(j,1)
B(j,2)
B(j,3)
140
141
142
143
YS(j)
W(i,0)
W(i,1)
W(i,2)
W(i,3)
Y DEC
X DEC
X DEC
X DEC
X DEC
230
231
232
233
40
Ax(0) ~ Ax(nw-1)
330
331
332
333
502
YR(3)
AC(3)
YR(2)
AC(2)
YR(1)
AC(1)
504
YR(0)
AC(0)
503
500

FIG. 27

ADDRESS		COMPARED / NOT COMPARED			
ROW ADDRESS	$A_X(0)$	○	×	×	×
	$A_X(1)$	○	○	×	×
	$A_X(2)$	○	○	×	×
	⋮	⋮	⋮	⋮	⋮
	$A_X(n_W-3)$	○	○	×	×
	$A_X(n_W-2)$	○	○	○	×
	$A_X(n_W-1)$	○	○	○	×
COLUMN ADDRESS	$A_Y(0)$	○	○	○	○
	$A_Y(1)$	○	○	○	○
	$A_Y(2)$	○	○	○	○
	⋮	⋮	⋮	⋮	⋮
	$A_Y(n_B-3)$	○	○	○	○
	$A_Y(n_B-2)$	○	○	○	○
	$A_Y(n_B-1)$	○	○	○	○
NUMBER OF BITS REPLACED AT A TIME		1	2	$\frac{N_W}{4}$	N_W

○ : COMPARED

× : NOT COMPARED

FIG. 28

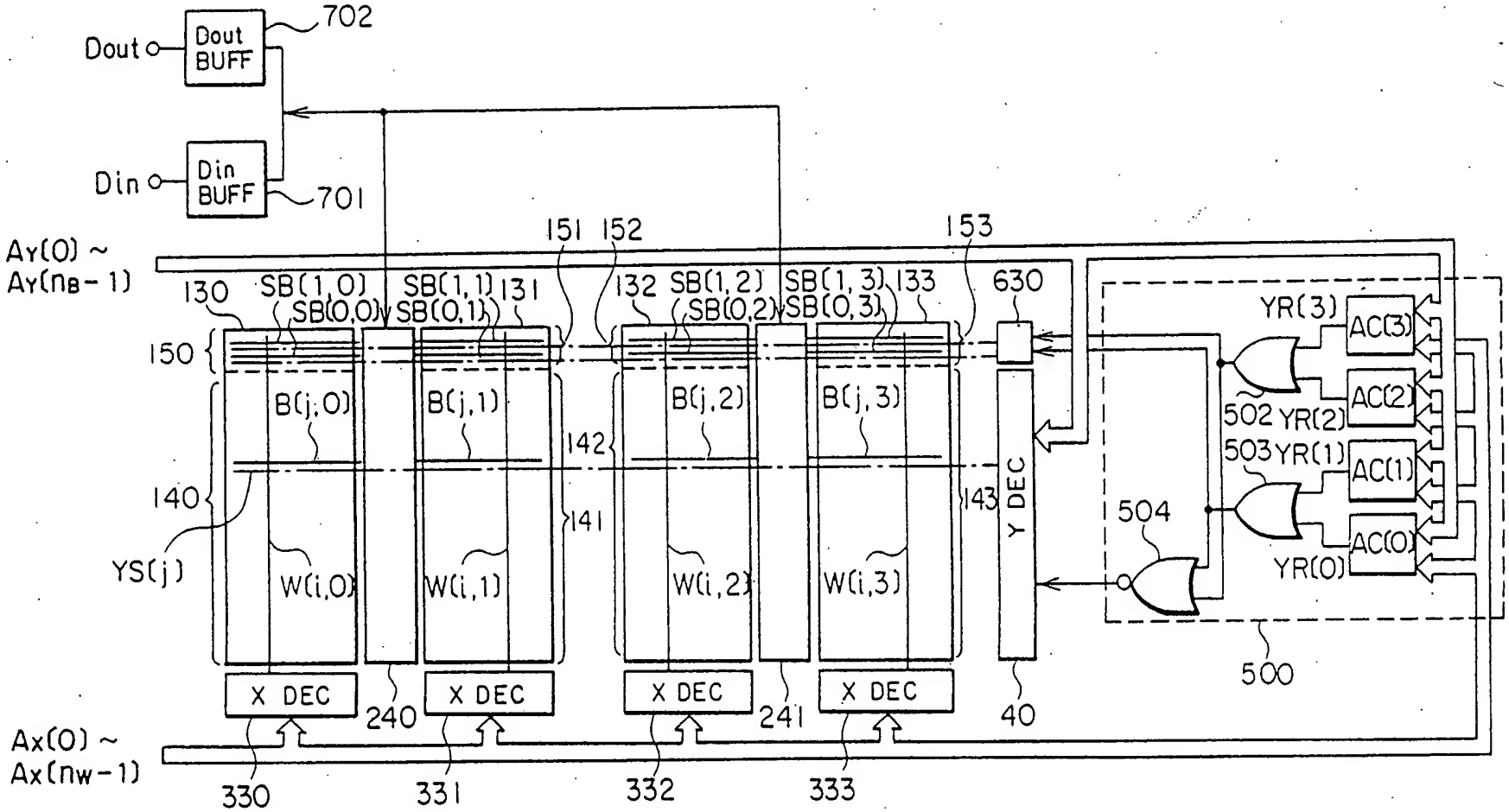

Dout
Dout BUFF
702
Din
Din BUFF
701
Ay(0) ~ Ay(nB-1)
151
152
153
130
SB(1,0)
SB(0,0)
SB(1,1)
SB(0,1)
131
132
SB(1,2)
SB(0,2)
SB(1,3)
SB(0,3)
133
630
150
B(j,0)
B(j,1)
B(j,2)
B(j,3)
142
140
141
143
Y DEC
YS(j)
W(i,0)
W(i,1)
W(i,2)
W(i,3)
YR(3)
AC(3)
502
YR(2)
AC(2)
503
YR(1)
AC(1)
504
AC(0)
YR(0)
500
X DEC
X DEC
X DEC
X DEC
240
241
40
Ax(0) ~ Ax(nw-1)
330
331
332
333

FIG. 29

ADDRESS		COMPARED / NOT COMPARED				
ROW ADDRESS	$A_X(0)$	○	×	×	×	×
	$A_X(1)$	○	○	×	×	×
	$A_X(2)$	○	○	×	×	×
	⋮	⋮	⋮	⋮	⋮	⋮
	$A_X(n_W-3)$	○	○	×	×	×
	$A_X(n_W-2)$	○	○	○	×	×
	$A_X(n_W-1)$	○	○	○	○	×
COLUMN ADDRESS	$A_Y(0)$	○	○	○	○	○
	$A_Y(1)$	○	○	○	○	○
	$A_Y(2)$	○	○	○	○	○
	⋮	⋮	⋮	⋮	⋮	⋮
	$A_Y(n_B-3)$	○	○	○	○	○
	$A_Y(n_B-2)$	○	○	○	○	○
	$A_Y(n_B-1)$	○	○	○	○	○
NUMBER OF BITS REPLACED AT A TIME		1	2	$\frac{N_W}{4}$	$\frac{N_W}{2}$	N_W

○ : COMPARED

× : NOT COMPARED

FIG. 30

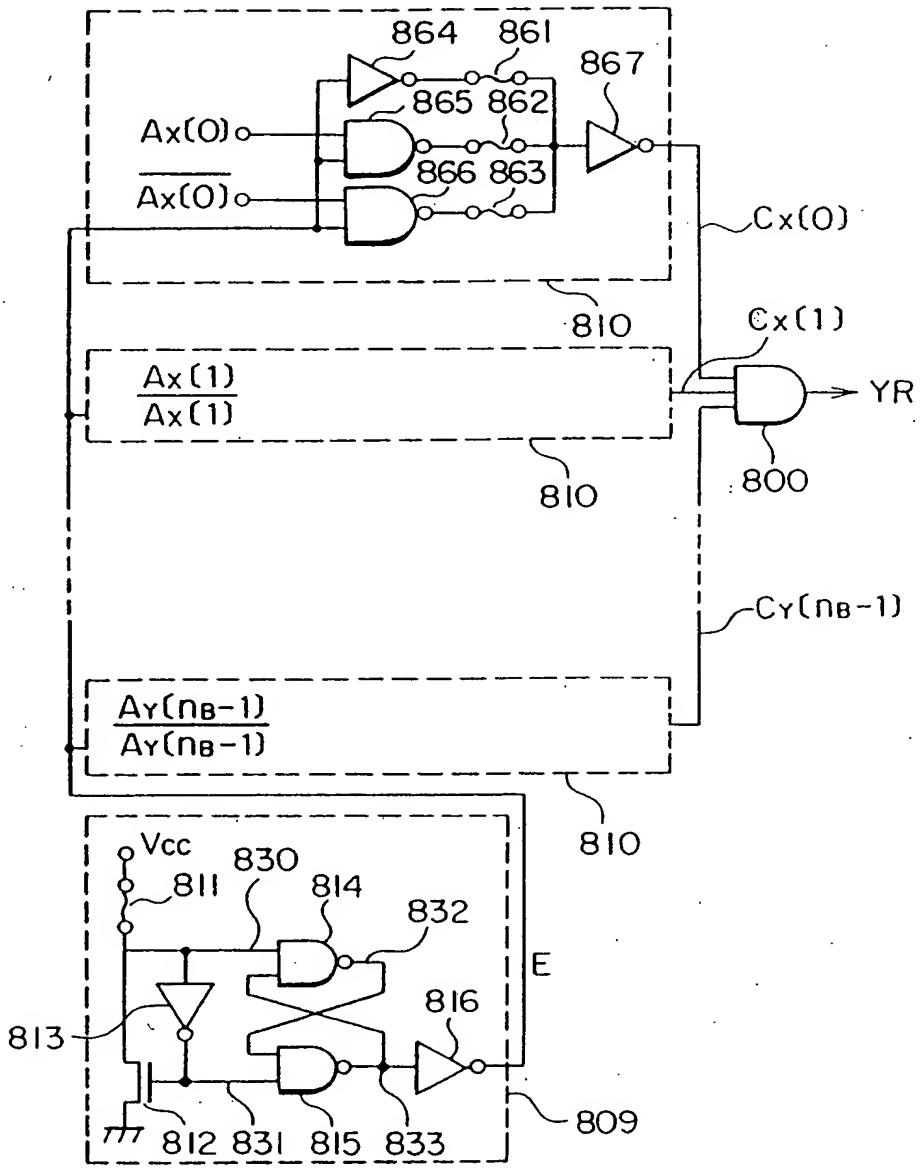

864
861
867
865
862
Ax(0)
866
863
Ax(0)
Cx(0)
810
Cx(1)
Ax(1)
Ax(1)
YR
810
800
Cy(nB-1)
Ay(nB-1)
Ay(nB-1)
810
Vcc
830
811
814
832
E
816
813
812
831
815
833
809

FIG. 31

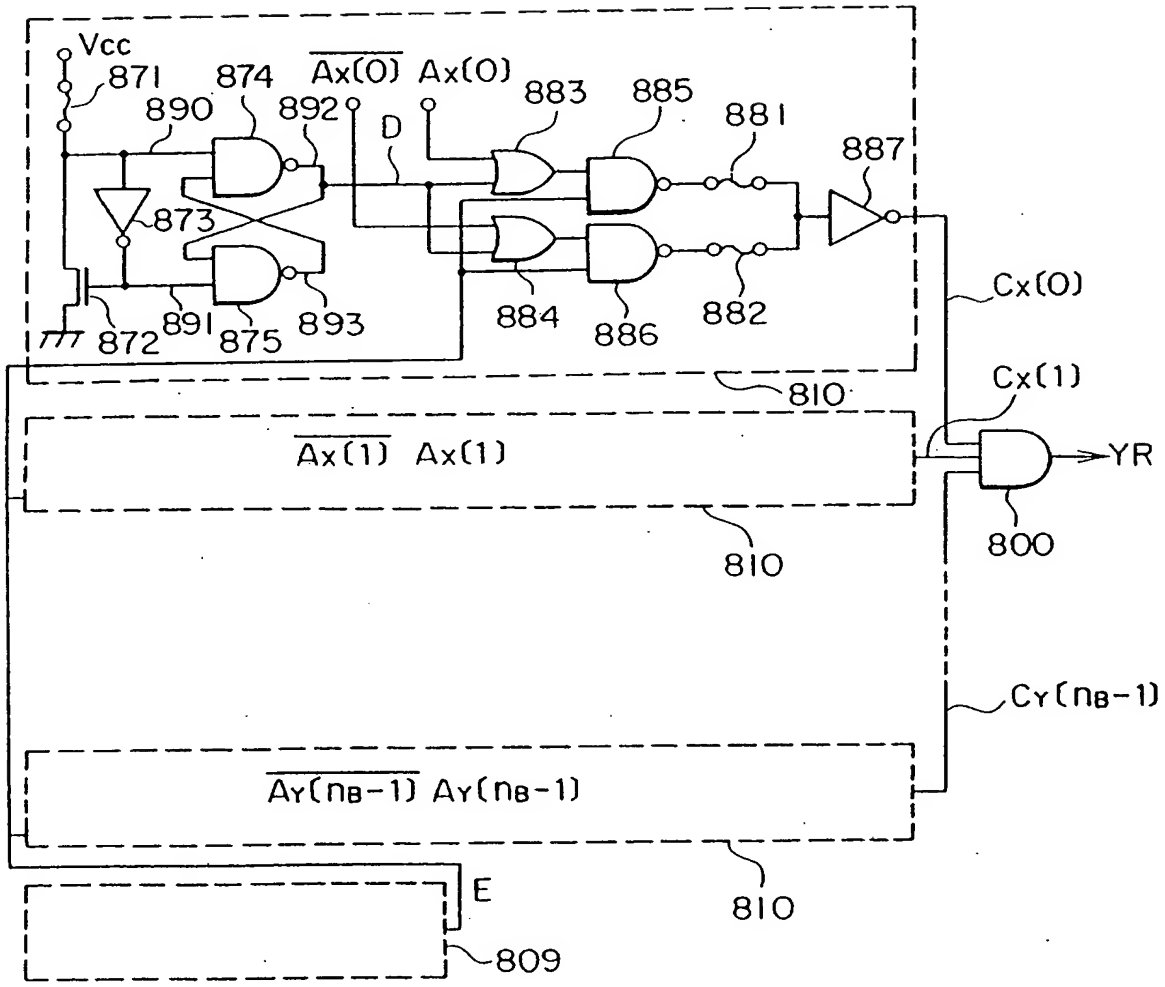
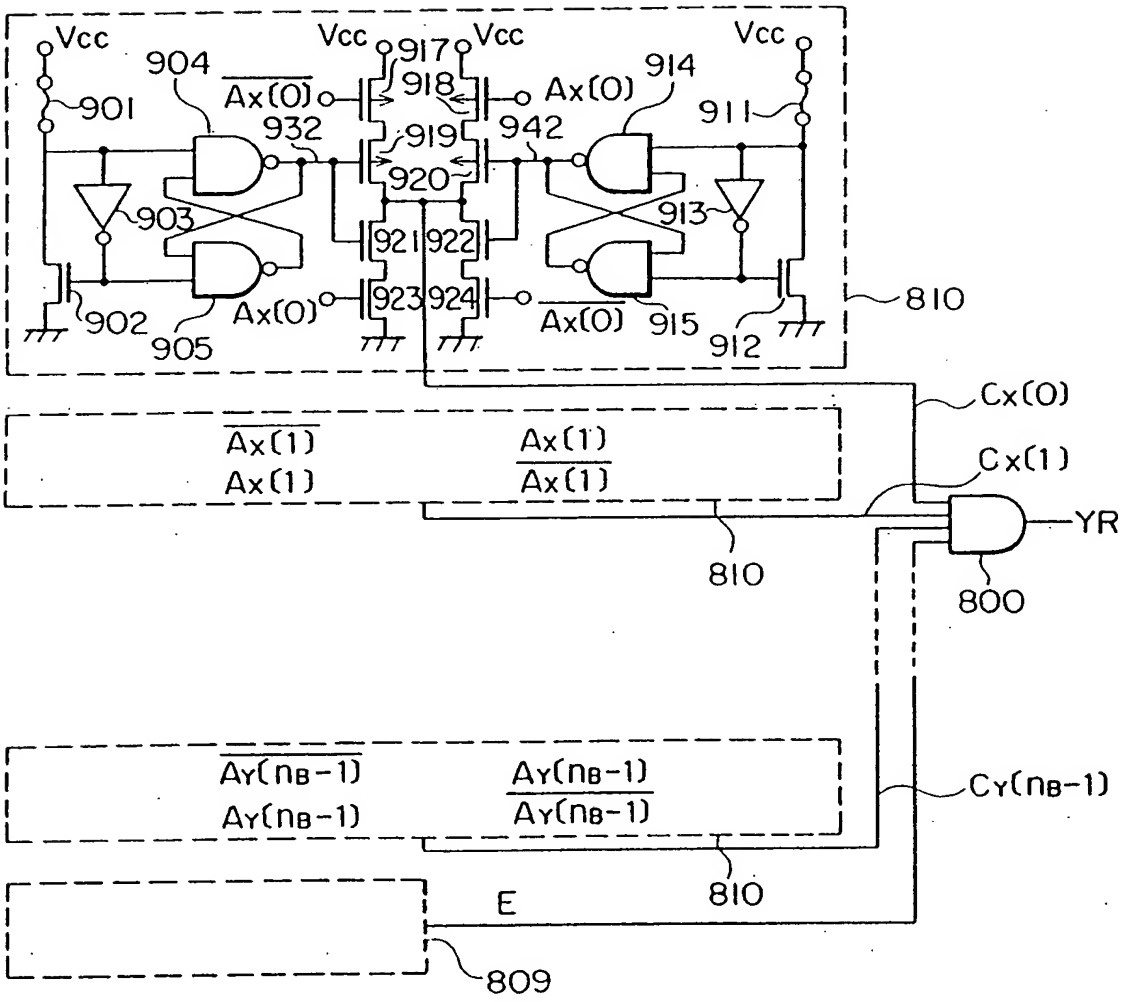

Vcc
871
874
$\overline{Ax(0)}$ Ax(0)
890
892
D
883
885
881
887
873
891
872
875
893
884
886
882
Cx(0)
810
Cx(1)
$\overline{Ax(1)}$ Ax(1)
YR
800
810
Cy(nB-1)
$\overline{Ay(nB-1)}$ Ay(nB-1)
810
E
809

FIG. 32


Vcc
Vcc
Vcc
Vcc
904
917
914
901
918
911
932
919
942
920
903
913
921
922
902
905
923
924
915
912
810
Cx(0)
Cx(1)
YR
800
810
E
809

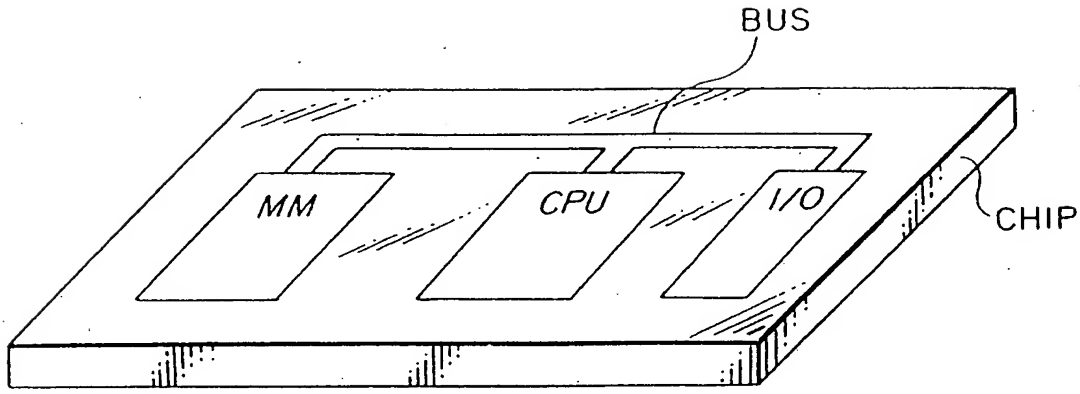



FIG. 33